

# EPC2040 – Enhancement Mode Power Transistor

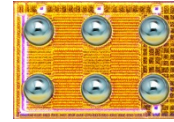
## Preliminary Specification Sheet



**Status:** Engineering

**Features:**

- $V_{DS}$ , 15V
- Maximum  $R_{DS(on)}$ , 28 m $\Omega$
- $I_D$ , 3.4 A
- Pulsed  $I_D$ , 28 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2040 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 0.85 mm x 1.20 mm

**Applications:**

- Pulsed Laser Driver
- LiDAR/Pulsed Power Applications

**MAXIMUM RATINGS**

Parameter	Value
Maximum Drain – Source Voltage	15 V
Gate – Source Maximum Voltage Range	-4 V < $V_{GS}$ < 6 V
Continuous Drain Current, ( $T_A = 25\text{ }^\circ\text{C}$ , $R_{\theta JA} = 210\text{ }^\circ\text{C/W}$ )	3.4 A
Maximum Pulsed Drain Current, 25 °C, $T_{pulse} = 300\text{ }\mu\text{s}$	28 A
Optimum Temperature Range	-40 °C < $T_J$ < 150 °C

**STATIC CHARACTERISTICS**

Parameter	Conditions	Value
Maximum Drain – Source Leakage	$V_{DS} = 12\text{ V}$ , $V_{GS} = 0\text{ V}$	0.25 mA
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 1.5\text{ A}$	28 m $\Omega$
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$ , $I_D = 1.5\text{ A}$	22 m $\Omega$
Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 1\text{ mA}$	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	1.2 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -4\text{ V}$	-0.25 mA

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated

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### DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
$C_{ISS}$ (Input Capacitance)	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$	100 pF
$C_{OSS}$ (Output Capacitance)		70 pF
$C_{RSS}$ (Reverse Transfer Capacitance)		25 pF
$Q_G$ (Total Gate Charge)	$V_{DS} = 6\text{ V}, I_D = 1.5\text{ A}, V_{GS} = 5\text{ V}$	930 pC
$Q_{GS}$ (Gate to Source Charge)	$V_{DS} = 6\text{ V}, I_D = 1.5\text{ A}$	270 pC
$Q_{GD}$ (Gate to Drain Charge)		160 pC
$Q_{G(TH)}$ (Gate Charge at Threshold)		200 pC
$Q_{OSS}$ (Output Charge)	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$	450 pC
$Q_{RR}$ (Source-Drain Recovery Charge)		0

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated

Specifications are with Substrate shorted to Source

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Figure 1: Typical Output Characteristics at 25°C

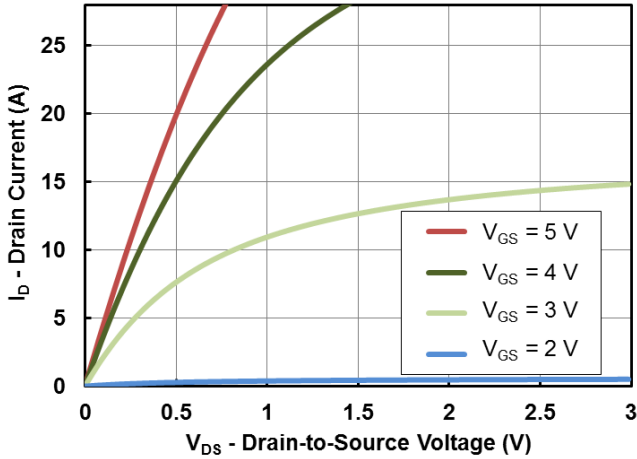


Figure 2: Transfer Characteristics

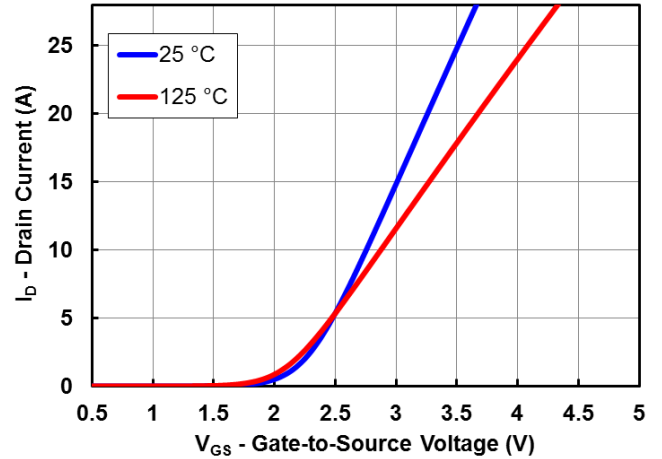


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

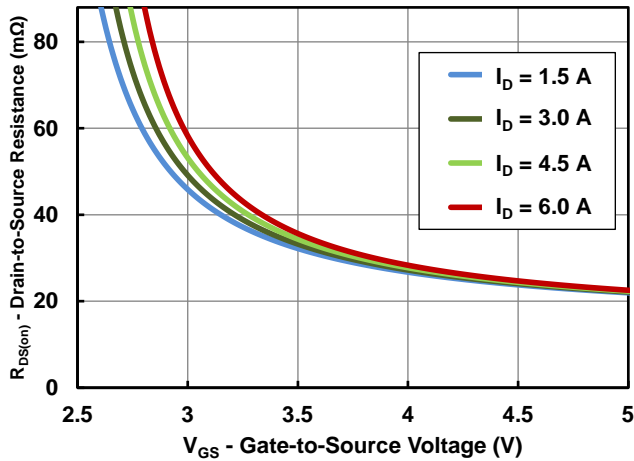


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Temperatures

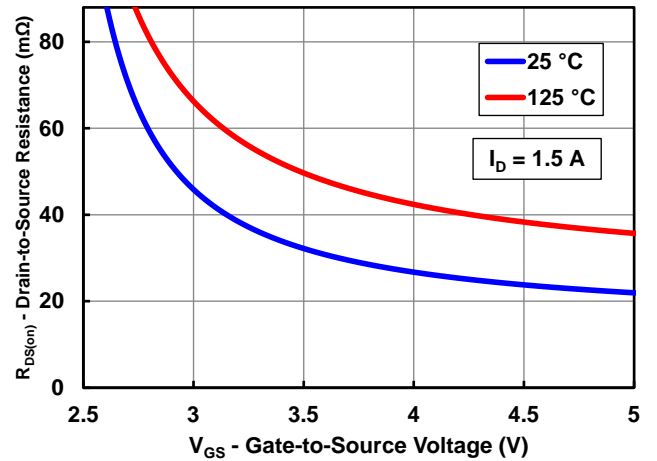


Figure 5a: Capacitance (Linear Scale)

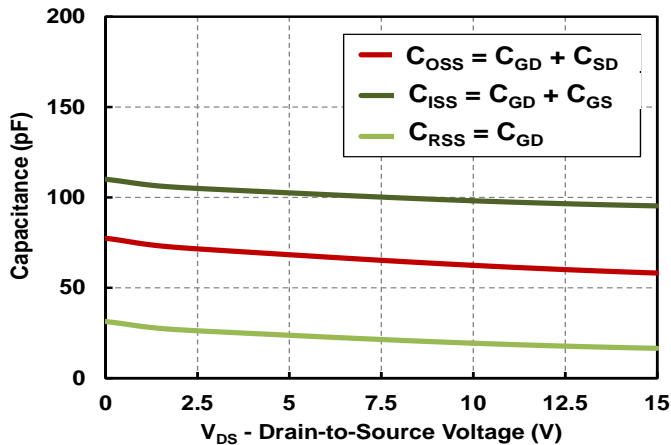
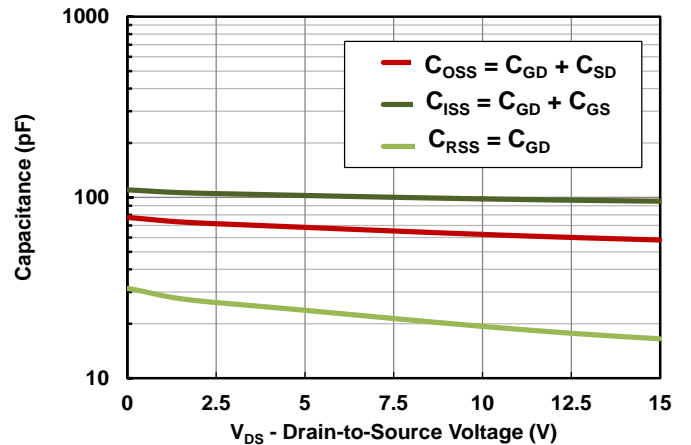


Figure 5b: Capacitance (Log Scale)



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Figure 6: Gate Charge

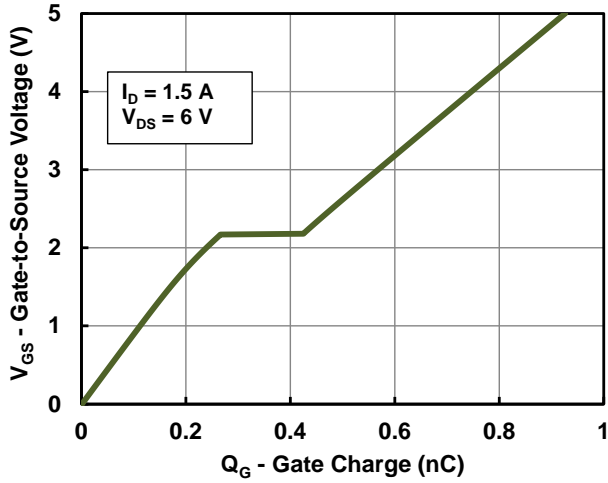


Figure 7: Reverse Drain-Source Characteristics

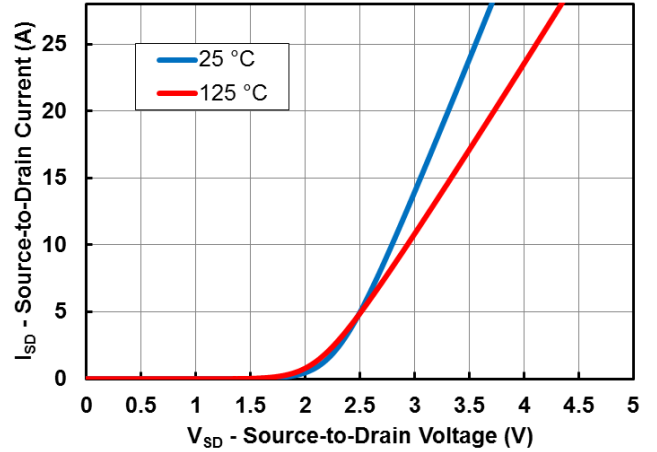


Figure 8: Normalized On Resistance vs. Temperature

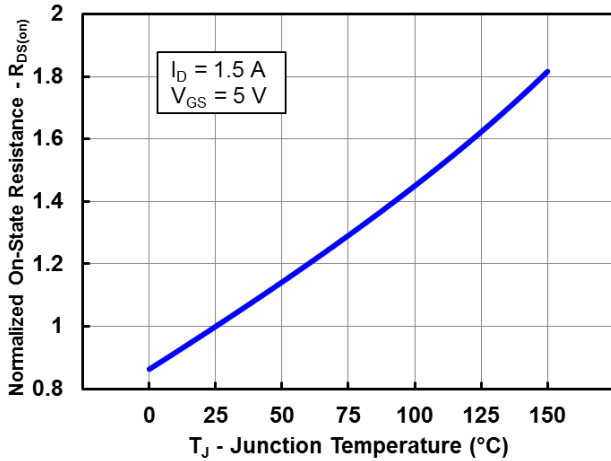


Figure 9: Normalized Threshold Voltage vs. Temperature

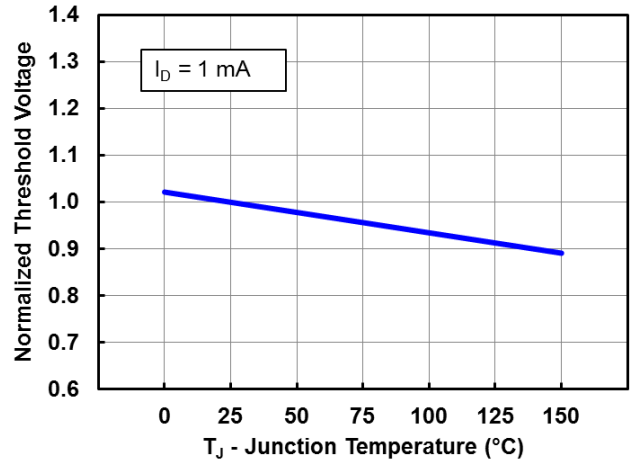
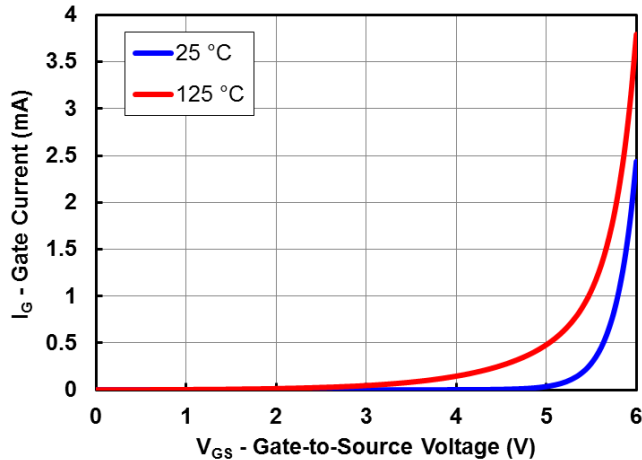


Figure 10: Gate-Source Characteristics



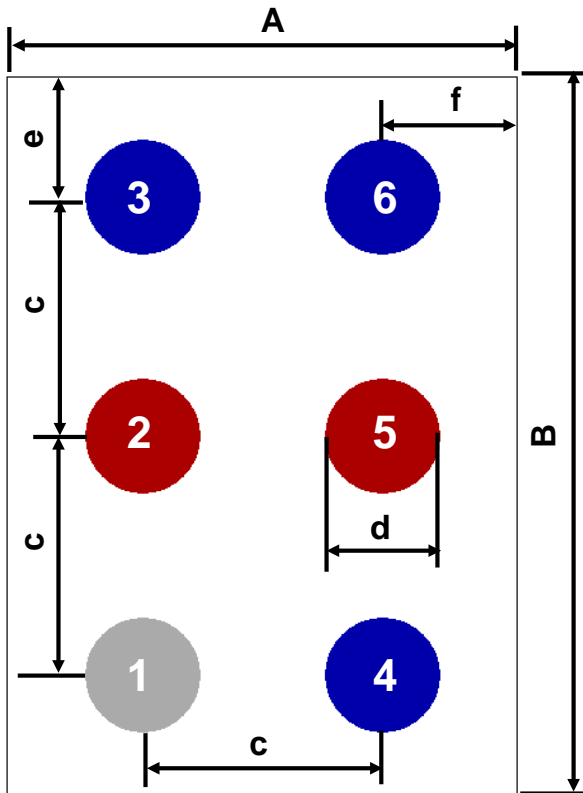
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### DIE OUTLINE

#### Solder Bar View



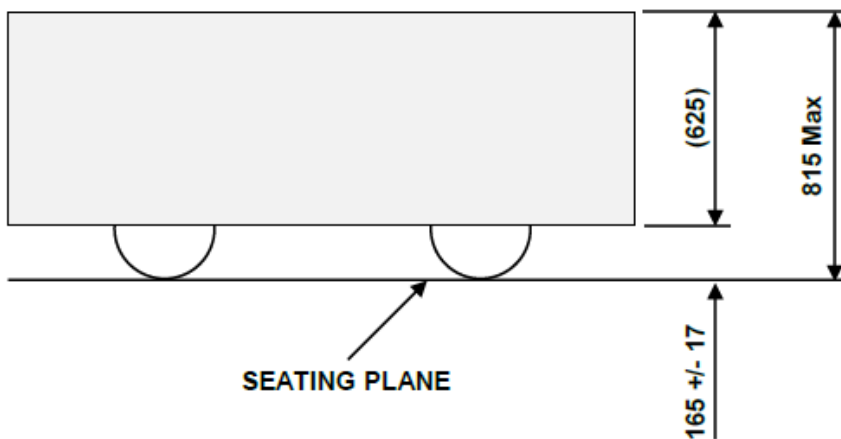
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	820	850	880
B	1170	1200	1230
c		400	
d	187	208	229
e	185	200	215
f	210	225	240

Pad 1 is Gate;

**Pads 2 & 5 are Drain;**

**Pads 3, 4, 6 are Source;**

#### Side View

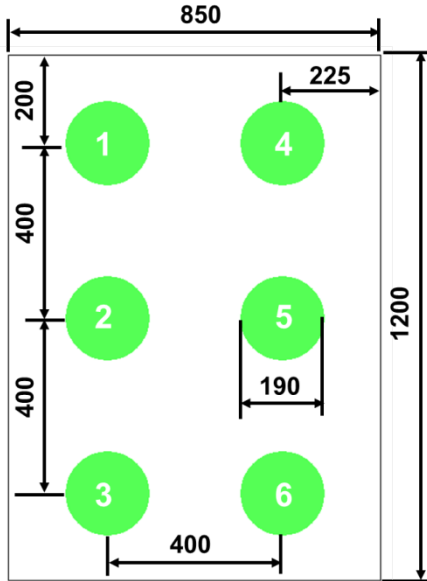


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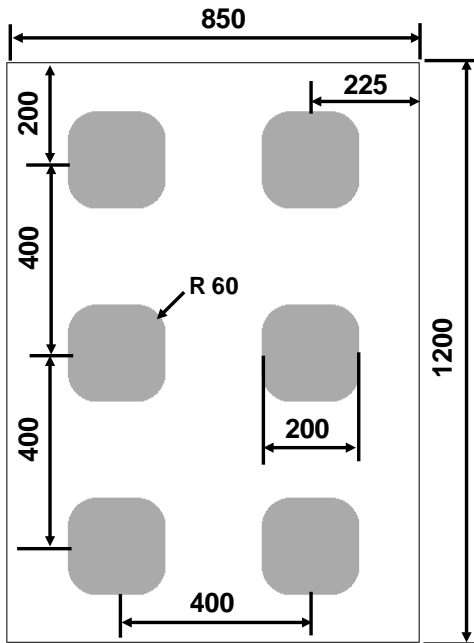
### RECOMMENDED LAND PATTERN

(Solder Mask Defined, Units in  $\mu\text{m}$ )



Pad 1 is Gate;  
 Pads 2 & 5 are Drain;  
 Pads 3, 4, 6 are Source;

### RECOMMENDED STENCIL DESIGN (Units in $\mu\text{m}$ )



Recommended stencil should be 4mil (100 $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

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