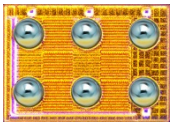
EPC2040 –Enhancement Mode Power Transistor
Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS}, 15V
- Maximum $R_{DS(on)}$, 28 mΩ
- I_D, 3.4 A
- Pulsed I_D, 28 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2040 eGaN® FETs are supplied only in passivated die form with solder balls

Die Size: 0.85 mm x 1.20 mm

Applications:

- Pulsed Laser Driver
- LiDAR/Pulsed Power Applications

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	15 V
Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
Continuous Drain Current, (T_A = 25 °C, $R_{\theta JA}$ = 210 °C/W)	3.4 A
Maximum Pulsed Drain Current, 25 °C, T_{pulse} = 300 µs	28 A
Optimum Temperature Range	-40 °C < T_J < 150 °C

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Leakage	V_{DS} = 12 V, V_{GS} = 0 V	0.25 mA
Maximum $R_{DS(on)}$	V_{GS} = 5 V, I_D = 1.5 A	28 mΩ
Typical $R_{DS(on)}$	V_{GS} = 5 V, I_D = 1.5 A	22 mΩ
Gate – Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	V_{GS} = 5 V	1.2 mA
Gate – Source Maximum Negative Leakage	V_{GS} = -4 V	-0.25 mA

T_J = 25 °C unless otherwise stated

DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C_{ISS} (Input Capacitance)	V_{DS} = 6 V, V_{GS} = 0 V	100 pF
C_{OSS} (Output Capacitance)		70 pF
C_{RSS} (Reverse Transfer Capacitance)		25 pF
Q_G (Total Gate Charge)	V_{DS} = 6 V, I_D = 1.5 A, V_{GS} = 5 V	930 pC
Q_{GS} (Gate to Source Charge)	V_{DS} = 6 V, I_D = 1.5 A	270 pC
Q_{GD} (Gate to Drain Charge)		160 pC
$Q_{G(TH)}$ (Gate Charge at Threshold)		200 pC
Q_{OSS} (Output Charge)	V_{DS} = 6 V, V_{GS} = 0 V	450 pC
Q_{RR} (Source-Drain Recovery Charge)		0

T_J = 25 °C unless otherwise stated
Specifications are with Substrate shorted to Source

Figure 1: Typical Output Characteristics at 25°C

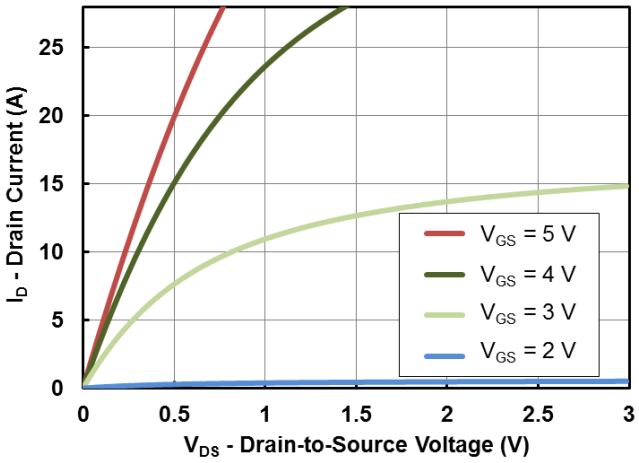


Figure 2: Transfer Characteristics

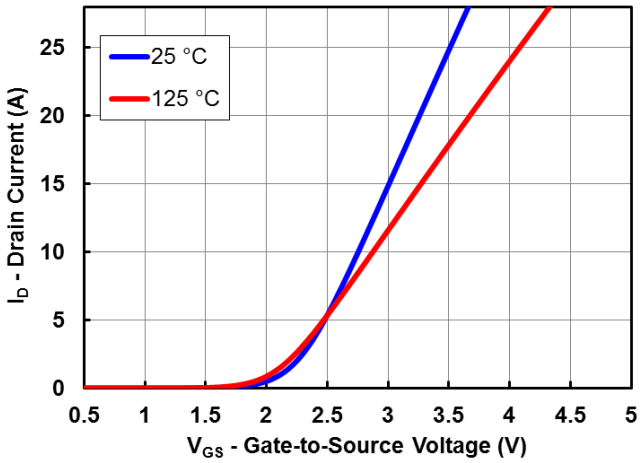


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

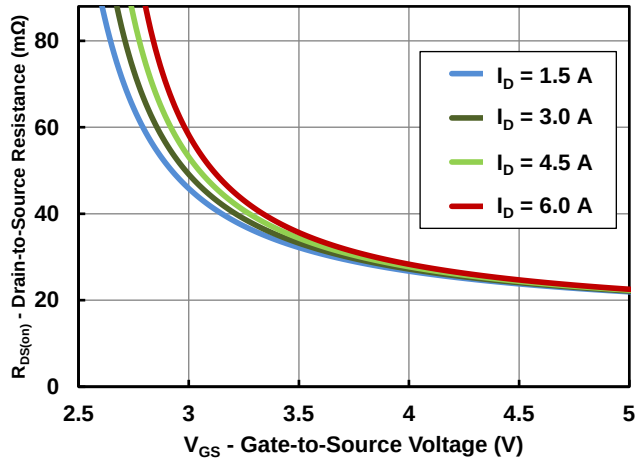


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Drain Temperatures

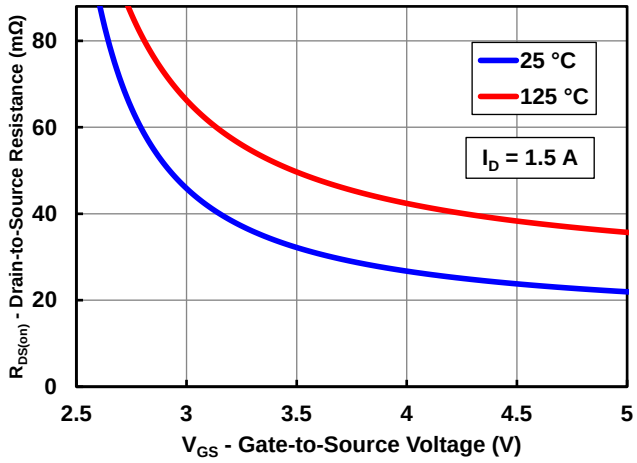


Figure 5a: Capacitance (Linear Scale)

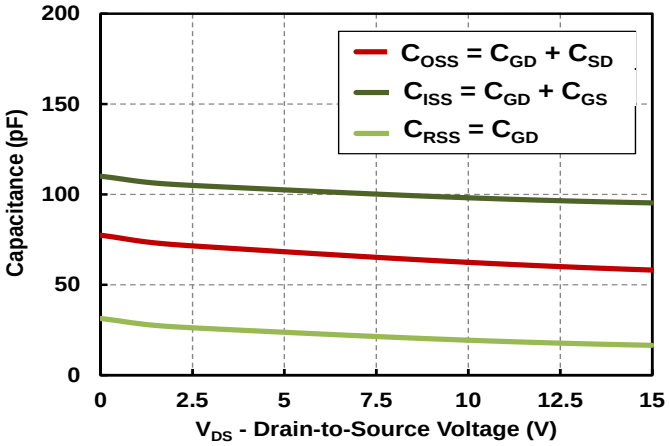


Figure 5b: Capacitance (Log Scale)

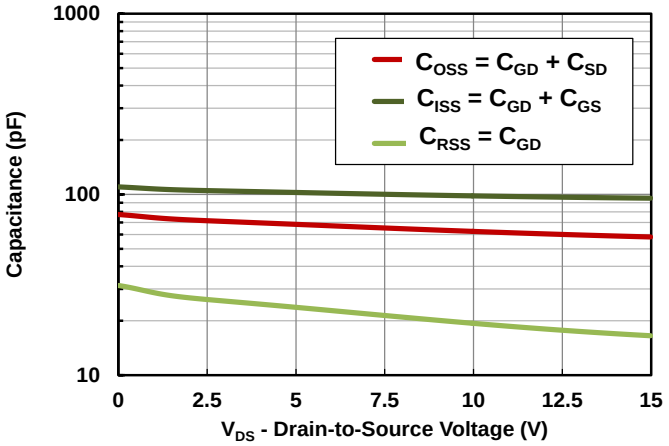


Figure 6: Gate Charge

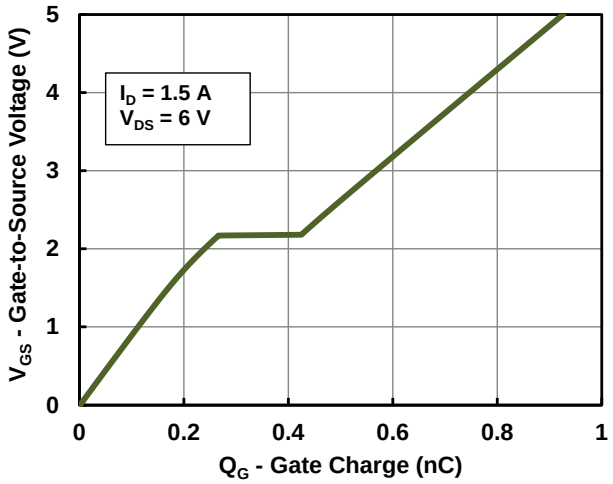


Figure 7: Reverse Drain-Source Characteristics

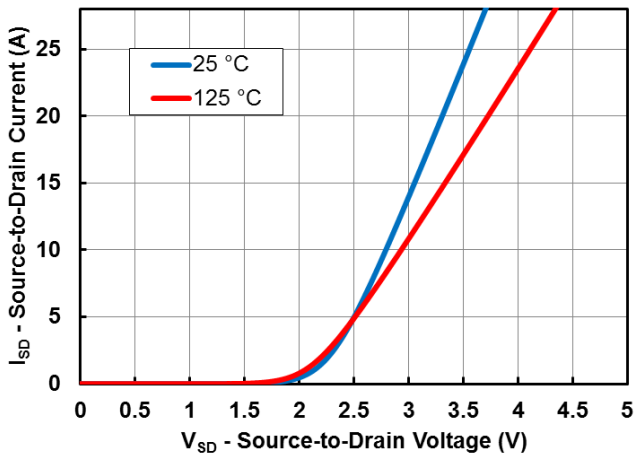


Figure 8: Normalized On Resistance vs. Temperature

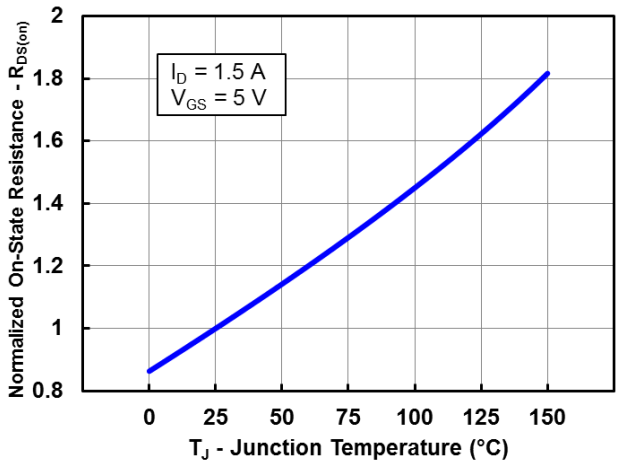


Figure 9: Normalized Threshold Voltage vs. Temperature

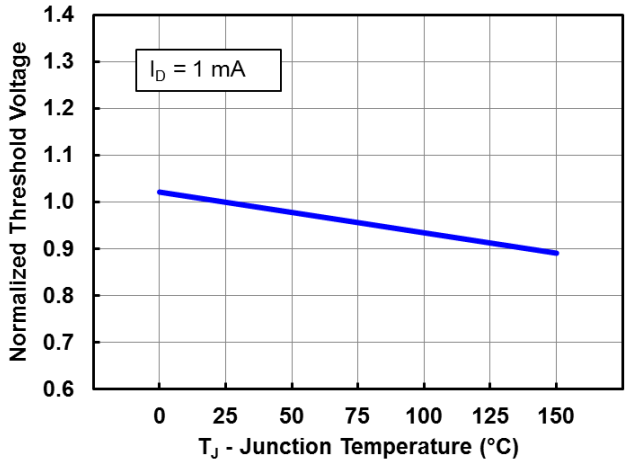
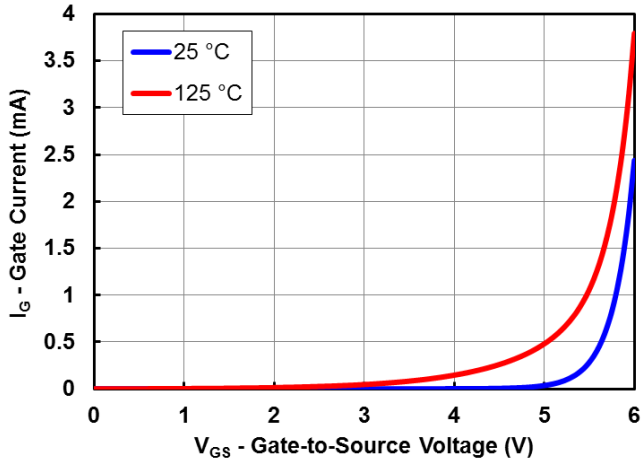
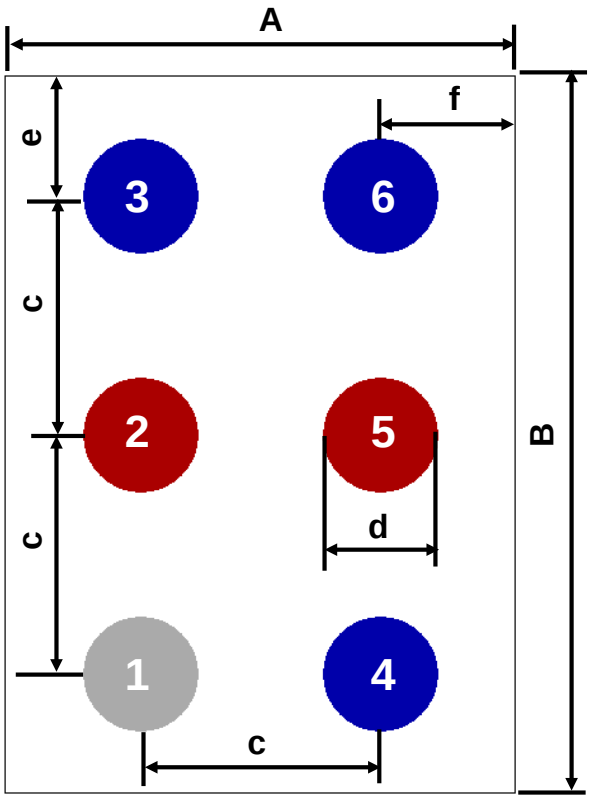


Figure 10: Gate-Source Characteristics



DIE OUTLINE

Solder Bar View



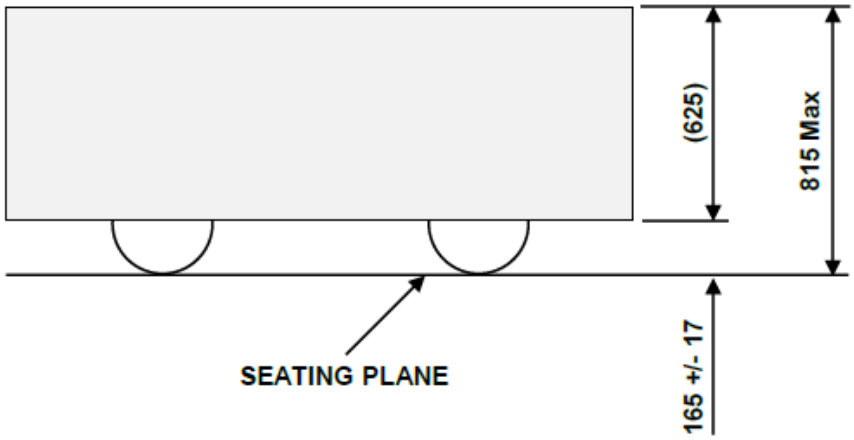
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	820	850	880
B	1170	1200	1230
c		400	
d	187	208	229
e	185	200	215
f	210	225	240

Pad 1 is Gate;

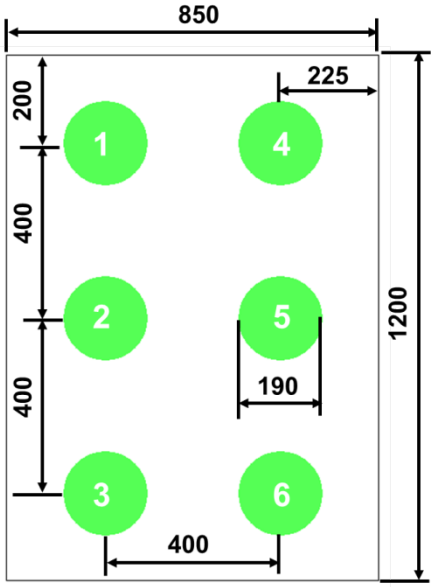
Pads 2 & 5 are Drain;

Pads 3, 4, 6 are Source;

Side View

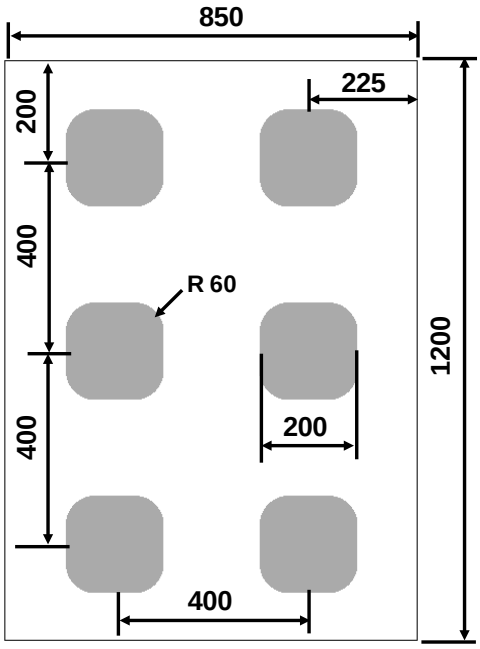


RECOMMENDED LAND PATTERN
(Solder Mask Defined, *Units in µm)*



Pad 1 is Gate;
Pads 2 & 5 are Drain;
Pads 3, 4, 6 are Source;

RECOMMENDED STENCIL DESIGN (*Units in µm)*



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Revised Janaury, 2016