MPC8360E PowerQUICC™ II Pro Family

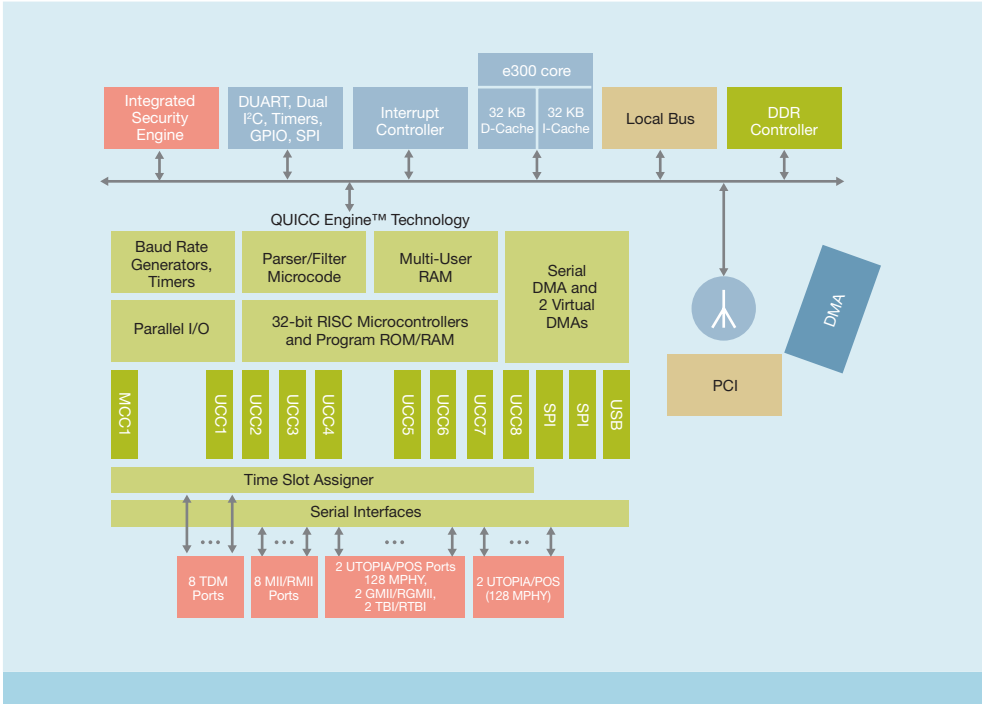
Overview

Freescale Semiconductor's MPC8360E PowerQUICC™ II Pro family of integrated communications processors is a next-generation extension of the popular PowerQUICC II line containing Power Architecture™ technology. The MPC8360E family incorporates a next-generation communications engine, the QUICC Engine™, supporting a wide range of protocols, including Gigabit Ethernet and OC-12 asynchronous transfer mode (ATM)/Packet over Sonet (POS). Additional enhancements include the e300 core, built on Power Architecture technology (an enhanced version of the 603e core with larger caches), scaling up to 667 MHz, up to two DDR memory controllers and the integrated security engine.

The MPC8360E PowerQUICC II Pro communications processor's advanced features make it suitable for today's and tomorrow's wired and wireless access equipment, as well as small and medium enterprise networking equipment. Target applications include multi-tenant units (MTUs), digital subscriber line access multiplexers (DSLAMs), wireless base stations, multi and fixed subscriber access nodes, add/drop multiplexers and routers.

The MPC8358E processor, a member of the MPC8360E PowerQUICC II Pro family, is pin-compatible with the MPC8360E. The MPC8358E offers a cost-effective, low-power processing solution that meets the performance requirements for broadband access applications such as small-to-medium enterprise (SME) routers, low-end DSLAMs and IP private automatic branch exchange (PABX) systems.

MPC8360E



e300 System-on-a-Chip Platform

The MPC8360E PowerQUICC II Pro family is based on the e300 system-on-a-chip (SoC) platform. This makes it easy and fast to add or remove functional blocks and develop additional SoC-based family members for emerging markets. At the heart of the e300 SoC platform is Freescale's e300 core, built on Power Architecture technology. The e300 core is an enhanced version of the 603e core used in previous-generation PowerQUICC II processors. Enhancements include twice as much L1 cache (32 KB data cache and 32 KB instruction cache) with integrated parity checking and other performance-enhancing features. The e300 core is software-compatible with existing 603e core-based products.

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Connectivity

The MPC8360E processor is designed to support a wide range of communications interfaces, such as MII, RMII, GMII, TBI, RTBI, NMSI, UTOPIA, POS and TDM. The dual 32-bit DDR memory controllers help to ensure high-speed memory access and a local system bus operating up to 133 MHz. Additional system connectivity is supplied by dual UART, dual inter-integrated circuit (I^2C), dual serial peripheral interface (SPI), PCI interfaces and Universal Serial Bus (USB) interface (USB 2.0 full/low speed compatible).

Integrated Security

The MPC8360E and MPC8358E processors feature integrated security with the powerfully integrated security engine derived from Freescale's security coprocessor product line. Integrated security supports DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms, as well as a public key accelerator and an on-chip random number generator. The integrated security engine is capable of single-pass encryption and authentication, as required by IPsec, the IEEE® 802.11i standard and other security protocols.

Typical Applications

- DSL infrastructure
  - DSLAMs
  - MTUs
- Wireless infrastructure
  - Base transceiver station (BTS)
  - Base station controller (BSC)
  - Radio network controller (RNC)
  - Node B
- Small and medium enterprise (SME) routers
  - Intrusion detection/protection system (IDS/IPS)
  - Secure VPN
  - Firewall
- Add/drop multiplexers and digital cross connects
- Integrated voice routers and digital IP-based private automatic branch exchange (PABX)
- Multi-service access nodes (MSAN)
- Industrial and general-purpose networking

QUICC Engine

Freescale's QUICC Engine technology includes two optimized RISC processors supporting a wide range of protocols while providing high data throughput of up to 1.2 Gbps. Flexibility is provided by the eight unified communications controllers (UCCs) providing support for Fast Ethernet, Gigabit Ethernet, high-level data link control (HDLC) and ATM/POS at up to OC-12 speeds. The MPC8360E and MPC8358E support connectivity up to eight T1/E1s. The MPC8360E supports eight TDMs and the MPC8358E supports four TDMs, with each TDM capable of supporting a clear channel T3/E3. One multi-channel communications controller (MCC) on the MPC8360E supports up to 256 x 64 kbps HDLC or transparent channels.

To simplify the transition from current PowerQUICC designs, the advanced QUICC Engine technology maintains a high degree of software compatibility with previous-generation PowerQUICC processor-based designs. This helps ease migration issues, reduce development costs and speed time to market.

The QUICC Engine technology builds upon the PowerQUICC shrink-wrapped software protocol support and provides enhancements in terms of interworking, parsing, switching and forwarding. A full set of configurable driver software and initialization support will also be available.

Interworking

With the potential to offer three revenue streams from a single IP packet network, the triple play of voice, video and data is the goal of every telecom operator. IP is the key enabler, and in time, it will be universal. Until then, equipment has to interoperate between circuit- and packet-switched networks and between many standards and protocols. The interoperability between standard protocols is referred to as interworking.

The QUICC Engine block supports ATM-to-Ethernet interworking without CPU intervention in support of the industry-standard RFC2684 specification. In addition, it can support MC/MLPPP to Ethernet interworking.

It is able to perform powerful table lookup functions including multiple fields from Layers 2 to 4 without CPU intervention.

Key Advantages

- High-performance, low-power and cost-effective communications processor solution
  - Convergence for packet-based networks
  - Compatibility with current PowerQUICC offerings
  - Cost-effective solution at the chip and system level
- Advanced QUICC Engine technology supporting a wide range of protocols and associated interworking
- DDR memory support—one 64-bit or 2 x 32-bit interfaces
- Low risk when transitioning from legacy to IP-based systems
- Quick to market enabled by software compatibility
- Low bill of material (BOM) cost

Product Family Highlights

- e300 core, built on Power Architecture technology (enhanced version of the 603e core with larger caches)
- DDR memory controller, 1 x 32/64-bit or 2 x 32-bit, up to 333 MHz
- QUICC Engine technology with eight communications interfaces supporting Fast Ethernet, Gigabit Ethernet, ATM, POS, HDLC, asynchronous HDLC, UART and transparent
- 32-bit PCI interface
- 32-bit local bus interface
- Optional integrated security

Technical Specifications

- e300 Power Architecture core operating from 266 MHz to 667 MHz
  - 32-bit, high-performance superscalar core
  - 1,261 MIPS at 667 MHz; 503 MIPS at 266 MHz
  - Double-precision floating point, integer, load/store, system register and branch processor units
  - 32 KB data and 32 KB instruction cache with line-locking support
- QUICC Engine technology initially operating up to 500 MHz
  - Two 32-bit RISC controllers for flexible support of the communications peripherals
  - Serial DMA channel for receive and transmit on all serial channels
  - QUICC Engine peripheral request interface for Integrated Security, PCI, IEEE Std 1588™
  - Eight UCCs supporting the following protocols and interfaces:
    - 10/100/1000 Mbps Ethernet
    - IEEE Std 1588 protocol supported
    - ATM SAR supporting AAL5, AAL2, AAL1, AAL0, TM 4.0 CBR, VBR, UBR traffic types, up to 64 KB external connections
    - Inverse multiplexing for ATM (IMA)
    - POS up to 622 Mbps
    - Transparent
    - HDLC
    - Multi-link, multi-class PPP
    - HDLC bus
    - UART
    - BISYNC
  - One multi-channel communications controller (MCC), supporting:
    - 256 TDM channels
    - Transparent and HDLC mode per channel
    - Support for Signaling System Number 7 (SS7)
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
  - Two UTOPIA/POS interfaces supporting up to 128 multi-PHY each
  - Two serial peripheral interfaces (SPIs)
  - Eight TDM interfaces, supporting:
    - Aggregate bandwidth of 64 kbps and 256 channels
    - Maximum of 16 Mbps and 256 channels on a single TDM link
    - 2,048 bytes of SI RAM (1,024 entries)
    - Eight programmable strobes
    - Bit or byte resolution
    - Independent transmit and receive routing, frame synchronization
    - T1, CEPT, T1/E1, T3/E3, pulse-code modulation highway, ISDN primary/basic rate, Freescale interchip digital link (IDL) and user-defined TDM serial interfaces
  - 16 independent baud rate generators
  - Four independent 16-bit timers that can be interconnected as two 32-bit timers
  - Two SPI ports that can be configured as an Ethernet management port for management data input/output (MDIO), while the other can be configured for cost-efffective serial peripherals; the SPI also has a CPU mode that can be configured by the CPU and not through the QUICC Engine
- USB interface (USB 2.0 full/low speed compatible)
- DDR memory controller
  - Programmable timing supporting DDR-1/2 SDRAM
  - 2 x 32-bit (MPC8360E only) or 1 x 32/64-bit data interface; up to 333 MHz data rate
  - Four banks of memory, each up to 1 GB
  - Full ECC support
- PCI interface
  - One 32-bit PCI 2.3 bus controller (3.3V I/O; up to 66 MHz)
- Integrated security (MPC8360E and MPC8358E only)
  - Public key execution (RSA and Diffie-Hellman)
  - Data encryption standard execution (DES and 3DES)
  - Advanced encryption standard (AES) execution
  - ARC-4 execution (RC4-compatible algorithm)
  - Message digest execution (SHA, MD5, HMAC)
  - Random number generation (RNG)
- Local bus controller
  - Multiplexed 32-bit address and data operating up to 133 MHz
  - 32-, 16- and 8-bit port sizes controlled by on-chip memory controller
- Dual UART (DUART)
- Dual I^2C interfaces (master or slave mode)
- Four-channel DMA controller
- General-purpose parallel I/O
- IEEE 1149.1 JTAG test access port
- Package option: 37.5 mm X 37.5 mm 740 TBGA (MPC8360E, MPC8358E); 29 mm x 29 mm 668 PBGA (MPC8358 only)
- Process technology: 130 nm CMOS
- Voltage: 1.2V core voltage with 3.3V, 2.5V and 1.8V I/O

MPC8360e Family Features Comparison	MPC8358E	MPC8360E
CPU	e300	e300
• I-Cache/D-Cache (KB)	32/32	32/32
• Available clock frequencies	Up to 400 MHz	Up to 667 MHz
QUICC Engine™	2 x RISC core	2 x RISC core
• Available clock frequencies	Up to 400 MHz	Up to 500 MHz
• Ethernet	Up to 2 x 10/100/1000 Up to 6 x 10/100	Up to 2 x 10/100/1000 Up to 8 x 10/100
• ATM	1 x UTOPIA L2	2 x UTOPIA L2
○ MPHY	Single 31/128 port	128 per UTOPIA port
• POS	Yes	Yes
• TDM	Up to 4 TDM interfaces Up to 256 channels at 16 Mbps on a single interface Up to 4 clear channel T3/E3	Up to 8 TDM interfaces Up to 256 channels at 16 Mbps on a single interface Up to 8 clear channel T3/E3
Memory controller	1 x 32/64-bit DDR-1/2	1 x 32/64-bit or 2 x 32-bit DDR-1/2
Local bus	Yes	Yes
PCI	One 32-bit (up to 66 MHz)	One 32-bit (up to 66 MHz)
Integrated security engine*	Yes	Yes
DUART	Yes	Yes
I^2C controller	2	2
SPI	2	2
USB	Yes	Yes
Interrupt controller	Yes	Yes
Package options	740 TBGA 668 PBGA	740 TBGA

*"E" in the product name designates encryption acceleration through an integrated security engine. MPC8360 and MPC8358 processor versions without integrated security engines are available.

Learn More: For more information about the MPC8360E Family and other Freescale communications processor products, please visit **www.freescale.com/powerquicc**.

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